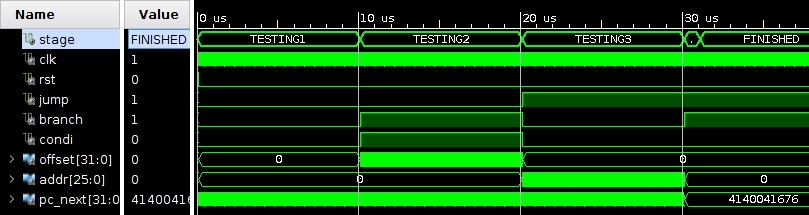
PC functional simulation

PC has 4 different source:

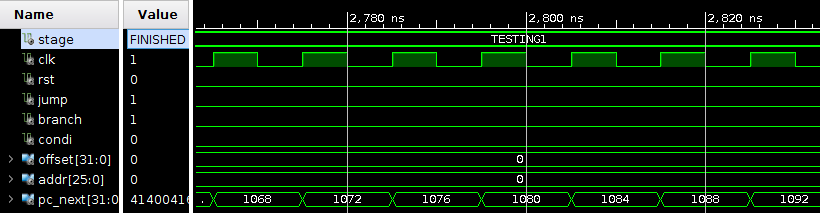
1. Continuously increasing: nextPC = PC + 4
2. Branch instruction: nextPC = PC + 4 + offset\*4
3. Jump instruction: nextPC = (PC+4)[31:28] & addr & “00”
4. Halt instruction: nextPC = PC

For each situation, I tested the PC unit on 1000 random cases and used ‘assert’ statement to check the output automatically (see tb\_pc.vhd for details). The stage signal would change to FINISH only when all test cases passed, otherwise, the simulation would stop with severity level ‘failure’.

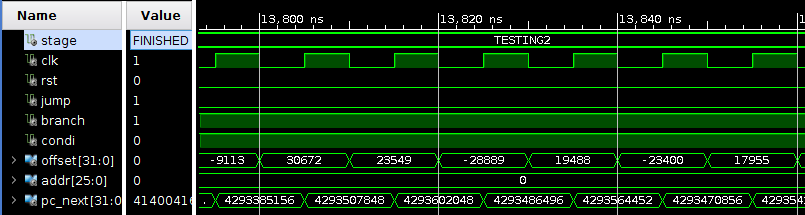
Functional simulation:



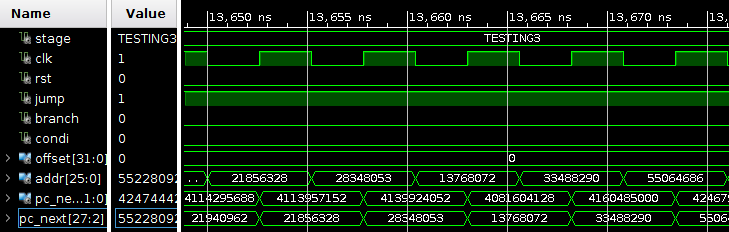
▲ Signal wave overview. All cases passed.



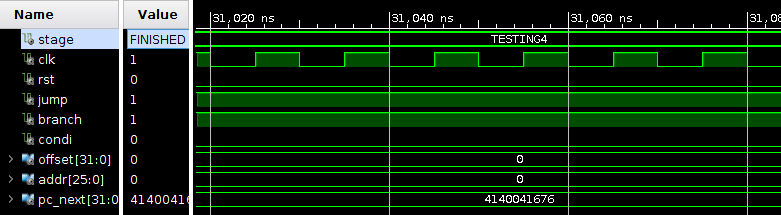
▲ Testing continuously increasing



▲ Testing branch instruction

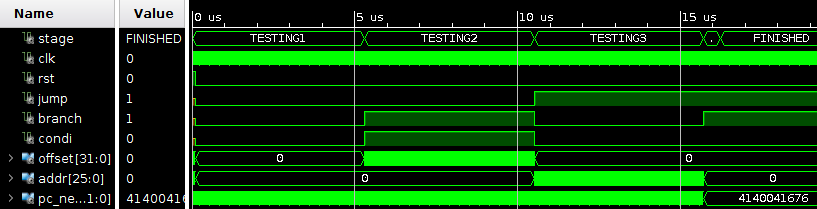


▲ Testing jump instruction

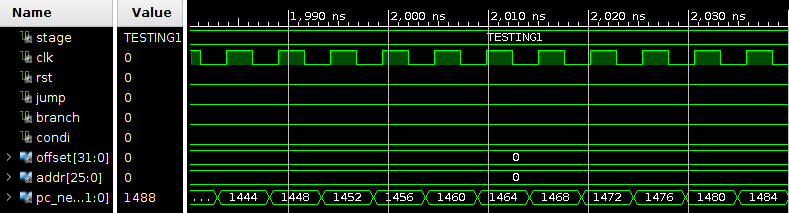


▲ Testing halt instruction

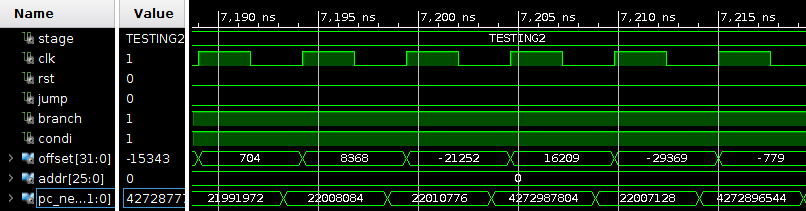
Timing simulation:



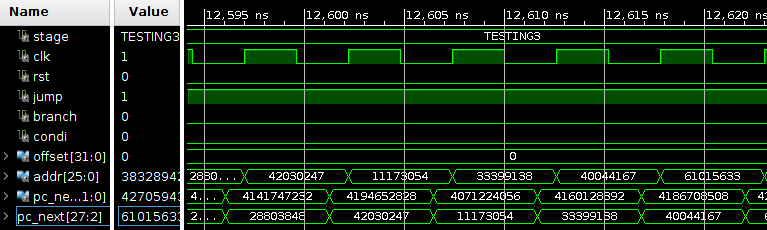
▲ Signal wave overview. All cases passed.



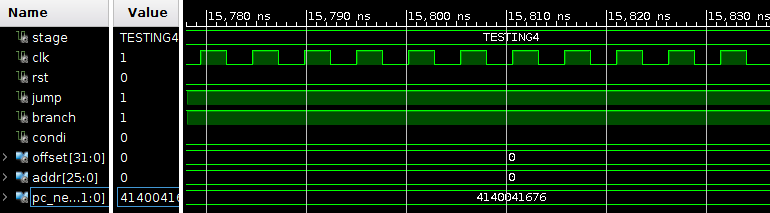
▲ Testing continuously increasing



▲ Testing branch instruction



▲ Testing jump instruction



▲ Testing halt instruction

Highest clk frequency:

Critical path delay = 5.166 ns

CLK frequency = 193.6 ns